Code: 13A04303 R13

B.Tech II Year I Semester (R13) Supplementary Examinations June 2015

SWITCHING THEORY AND LOGIC DESIGN

(Common to ECE & EIE)

Time: 3 hours Max. Marks: 70

PART - A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Find the complement of the function $F = A + BC$ and show that $F.\overline{F} = 0$.

(b) Perform the subtraction operation on 22-7 using 2's complement form.

(c) Convert the expression $f(A,B,C) = (A+B)(B+C)(A+C)$ in standard POS form.

(d) Simplify $\overline{\overline{A}B + \overline{A} + AB}$.

(e) Obtain the prime implicates for given Boolean expression. $f(A,B,C) = \sum(0,1,3,5,7)$ using k-map.

(f) Design a 4 bit parallel adder using Full adders.

(g) Explain how decoder can be converted into a demultiplexer with a neat block diagram.

(h) Compare PROM, PLA & PAL.

(i) Compare level and edge triggering.

(j) Assume that the 5 bit binary counter starts in the 0000 state then what will be the count after 144 input pulses.

PART - B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT - I

2 Encode the decimal number 365 in
(i) Binary (ii) BCD (iii) ASCII (iv) Excess – 3.

OR

3 Given the 8 – bit data word 01011011 generate the 12 bit composite word for the hamming code that corrects and detects single errors.

UNIT - II

4 (a) Implement the Boolean expression for Ex-OR gate using NAND gates.

(b) Simplify the Boolean expression $\overline{A}B\left(\overline{D} + \overline{C}D\right) + B(A + \overline{A}CD)$ to one literal.

OR

5 (a) Implement Ex- NOR gate using only NOR gates.

(b) Use the K-map method to simplify the following 5-variable function
$F = \sum(3,6,7,8,10,12,14,17,19,20,21,24,25,27,31)$

UNIT - III

6 (a) What is a decoder? Construct 3×8 decoder using logic gates and also write truth table.

(b) Design a 4 bit odd parity generator. Mentions its truth table.

OR

7 (a) Implement the following Boolean function using 8:1 multiplexer.
$F(A,B,C,D) = \overline{A}B\,\overline{D} + ACD + \overline{B}CD + \overline{A}\,\overline{C}D$

(b) Design a 2 bit comparator using gates.

UNIT - IV

8 (a) Construct a JK flip-flop using D flip-flop, 2×1 multiplexer and an inverter.

(b) Convert SR flip – flop to T flip – flop.

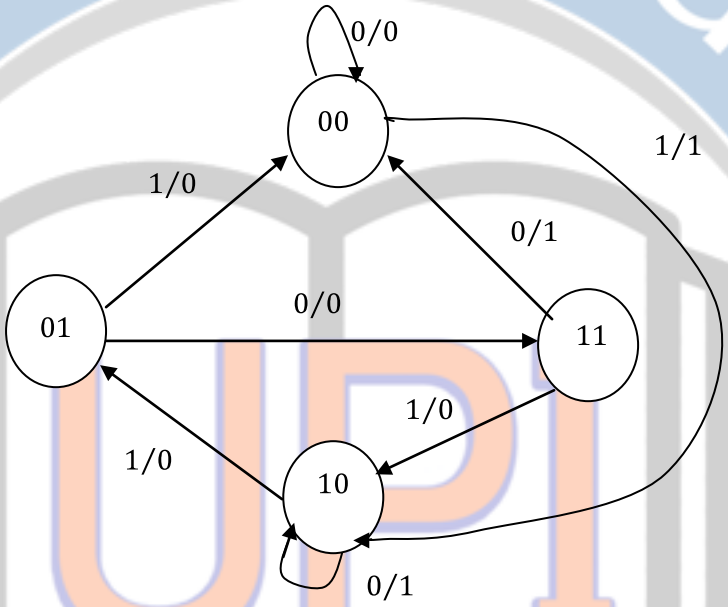
OR

9 Define the following terms in connection with a flip-flop
(i) Setup time (ii) Hold time (iii) Propagation delay time (iv) Preset (v) Clear.

Contd. in page 2

UNIT – V

10 A sequential circuit has one input and one output. The state diagram is shown below:



Design the sequential circuit with (a) D flip-flop (b) RS flip-flop (c) JK flip-flop.

OR

11 (a) Implement the following Boolean function using PLA

$F_1(w.x.y.z) = \sum(0,1,3,5,9,13)$

$F_2(w,x,y,z) = \sum(0,2,4,5,7,9,11,15)$

(b) What is hazard in switching circuits? Explain the design of hazard free switching circuit with an example.

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