Code: 13A04701 **R13**

B.Tech IV Year I Semester (R13) Regular Examinations November/December 2016

VLSI DESIGN

(Common to ECE & EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Distinguish between CMOS and BiCMOS.
(b) Describe the different operating regions for an MOS transistor.
(c) Define Sheet resistance of the MOS device.
(d) What are the limitations of scaling?
(e) Write short notes on switch logic.
(f) What are the different ways to improve clock distribution?
(g) What is parity generator?
(h) What are the advantages and applications of FPGA?
(i) What are the different types of modelling in VHDL?
(j) What is the need for testing?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Explain clearly about n-well CMOS fabrication process with neat diagrams.

OR

3 (a) Draw the V-I characteristics of MOSFET and prove that I_{ds} is linear function of V_{ds}.

(b) When the gate to source voltage V_{GS} of a MOSFET with threshold voltage of 400mv, working in saturation is 900mv, the drain current is observed to be 1mA and assuming that the MOSFET is operating at saturation, calculate the drain current for an applied V_{GS} of 1400mv.

UNIT – II

4 (a) Define fan-in and fan-out. Explain their effects on propagation delay.

(b) What do you mean by inverter delay? Explain.

OR

5 Draw a stick diagram for two input n-MOS NAND and NOR gates.

UNIT – III

6 Write short notes about the following:

(a) Pseudo nMOS logic
(b) Domino-Logic

OR

7 Discuss about the floor planning.

UNIT – IV

8 Explain the working principle of 6-transistor Static RAM and 1-transistor Dynamic RAM with necessary diagrams.

OR

9 (a) Draw and explain the architecture of a CPLD.

(b) Differentiate between the Full-custom and Semi-custom design.

UNIT – V

10 Explain the design capture and design verification tools.

OR

11 Explain the gate level and function level of testing.

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