

Code: 13A04303

R13

B.Tech II Year I Semester (R13) Supplementary Examinations June 2016

**SWITCHING THEORY & LOGIC DESIGN**

(Common to ECE and EIE)

Time: 3 hours

Max. Marks: 70

**PART – A**

(Compulsory Question)

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- 1 Answer the following: (10 X 02 = 20 Marks)
- (a) What is the BCD equivalent of 456?
  - (b) Draw the logic symbols of NAND and NOR gates.
  - (c) Write the advantages of Tabulation method over K-Map method.
  - (d) Write the given Boolean expression  $f = A+B$  in Sum of minterms.
  - (e) Define combinational logic design.
  - (f) Define the Decoder.
  - (g) Write the difference between Latch and Flip flop.
  - (h) List asynchronous inputs of a sequential device.
  - (i) List out list of PLDs.
  - (j) Write the difference between RAM and ROM.

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

- 2 Convert the given decimal number 234 to binary, quaternary, octal, hexadecimal and BCD equivalent.

**OR**

- 3 Perform the following:
- (i) Subtraction by using 10's complement for the given  $3456 - 245$ .
  - (ii) Subtraction by using 2's complement for the given  $111001 - 1010$ .

**UNIT – II**

- 4 Minimize the following Boolean function using k-map and realize using NAND Gates  $F(A, B, C, D) = \sum m(0, 2, 4, 6, 8, 10, 12, 14)$ .

**OR**

- 5 Minimize the given Boolean function  $F(A,B,C,D) = \sum m(0,1,2,3,6,7,13,15)$  using tabulation method and implement using basic gates.

**UNIT – III**

- 6 (a) Design 8X1 Multiplexer by using 4X1 Multiplexers.  
(b) Implement half adder using Decoder.

**OR**

- 7 Design a 4 bit adder cum subtractor using 1 bit full adders and explain.

**UNIT – IV**

- 8 (a) Design D Flip Flop by using SR Flip Flop and draw the timing diagram.  
(b) Write the differences between combinational and sequential circuits.

**OR**

- 9 (a) Draw the logic symbol, characteristics table and derive characteristics equation of JK flip flop.  
(b) Design T Flip Flop by using JK Flip Flop and draw the timing diagram.

**UNIT – V**

- 10 (a) Define asynchronous sequential design.  
(b) Implement the following Boolean functions  $F_1 = \sum m(0, 1, 2, 3, 8, 10, 12, 14)$ ,  $F_2 = \sum m(0, 1, 2, 3, 4, 6, 8, 10, 12, 14)$  using PAL.

**OR**

- 11 Draw and explain the construction of 4X3 RAM.

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