Code: 13A04303

R13

B.Tech II Year I Semester (R13) Regular & Supplementary Examinations December 2015

SWITCHING THEORY & LOGIC DESIGN

(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) State and prove De-Morgans theorem.
(b) What do you understand by universal gate?
(c) Convert the given equation Y=AB+AC'+BC into standard SOP form.
(d) Implement the following Boolean equation using only NAND gates Y=AB+CDE+F.
(e) Draw the logic diagram of full adder circuit and form the truth table.
(f) What is multiplier? Draw the block diagram of 4-input MUX.
(g) Give the comparison between combinational circuits and sequential circuits.
(h) What is shift register? Give the classification of them.
(i) What are the steps involved in designing an asynchronous sequential circuits?
(j) What are hazards in digital logic circuits? How it can be resolved?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Simplify the following Boolean expression: (i) F = (A+B)(A'+C)(B+C). (ii) F = A+B+C'+D(E+F)'

OR

3 (a) Expand the following Boolean functions F = xy+x'zin a standard product of maxterm form.
(b) Minimize the following Boolean function: f(A,B,C,D)=∑m(5,7,8,10,13,15)+∑d(0,1,2,3).

UNIT – II

4 (a) Simplify the following expression using the K-map for the 4-variable:
Y = AB'C+A'BC+A'B'C+A'B'C'+AB'C'
(b) Implement the following Boolean function using NOR gates Y=(AB'+A'B)(C+D').

OR

5 Simplify the Boolean function by using tabulation method.
F(a,b,c,d)=∑m(0,1,2,5,6,7,8,9,10,14)

UNIT – III

6 Discuss in detail about the design procedure for binary serial and parallel adder with diagram.

OR

7 Implement a 2-bit Magnitude comparator and write down its design procedure.

UNIT – IV

8 A sequential circuit with two D-flip flops A and B, two inputs 'x' and 'y' and one output 'z' is specified by the following next state and output equation.
A(t+1) = x'y+xA, B(t+1) = x'B+xA and Z = B
(i) Draw the logic diagram of the circuit. (ii) List the state table and draw the corresponding state diagram.

OR

9 Design and implement 3-bit ripple counter using J-K flip flop. Draw the state diagram, logic diagram and timing diagram for the same.

UNIT – V

10 What is critical and non-critical races in asynchronous circuits? How to avoid races? Illustrate with one example.

OR

11 Design and implement the following Boolean functions in PAL.

(a) A(w,x,y,z)=∑m(0,2,6,7,8,9,12,13)
(b) B(w,x,y,z)=∑m(0,2,6,7,8,9,12,13,14)
(c) C(w,x,y,z)=∑m(1,3,4,6,10,12,13)
(d) D(w,x,y,z)=∑m(1,3,4,6,9,12,14)

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