

B.Tech II Year I Semester (R13) Regular Examinations December 2014  
**SWITCHING THEORY & LOGIC DESIGN**  
 (Common to ECE and EIE)

Time: 3 hours

Max. Marks: 70

**PART – A**  
 (Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

- If  $143_5 = X_6$ , then X is.....
- Minimum number of two input NAND gates required to implement  $Y = A + B C$ .
- What is the importance of don't care conditions?
- SOP of  $F(x, y, z) = \sum(2, 3, 6, 7)$ .
- Implement OR gate using only two input NAND gates?
- Draw the block diagram of 2x4 decoder with enable.
- Draw the block diagram of sequential circuit using combinational circuit and memory unit.
- Draw the logic circuit of flip-flop and truth table using NOR gates.
- What is the function of EAROM?
- Mention few applications of PLA.

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

- Convert the following to Decimal and then to Octal. (i)  $4234_{16}$  (ii)  $10010011_2$
  - Implement the function with NOR-NOR logic  $Y = A C + B C + A B + D$ .
- Convert the following to Decimal and then to Hexadecimal. (i)  $1234_8$  (ii)  $11001111_2$
  - Find the complement of the following Boolean function and reduce into minimum number of literals.  
 $Y = BC' + A'D)(DB' + CD'$

**UNIT – II**

- Simplify the following Boolean expressions using K-map and implement them using NAND gates.  
 $F(W, X, Y, Z) = XZ + W'XY + WXY + W'YZ + W'YZ$
- Simplifying the following expression using tabulation technique.  
 $F = \sum m(0, 1, 2, 8, 9, 15, 17, 21, 24, 25, 27, 31)$

**UNIT – III**

- Design a 4 bit binary-to-Gray code converter.
  - Realize a 2-bit comparator.
- Design a 4 bit binary-to-BCD code converter.
  - Design 32:1 Mux using two 16:1 Muxs and one 2:1 Mux.

**UNIT – IV**

- Draw the circuit of JK flip flop using NAND gates and explain its operation.
  - Design a 2-input 2-output detector which produces an output 1 every time the sequence 0101 is detected. Implement the sequence detector using JK flip-flops.
- Convert S-R flip flop into JK-flip flop. Draw and explain the logic diagram.
  - A clocked sequential circuit with single input x and single output z produces an output  $z=1$  whenever the input x compares the sequence 1011 and overlapping is allowed. Obtain the state diagram, state table and design the circuit with D flip-flops.

**UNIT – V**

- Explain about ROM and PROM.
  - Design a BCD to excess-3 code converter using ROM.
- What is Race-free state Assignment? Explain.
  - Realize  $f = \sum m(0, 2, 3, 7, 9, 11, 15, 16)$  using ROM.

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