Code: 13A04306

R13

B.Tech II Year I Semester (R13) Regular Examinations December 2014

DIGITAL LOGIC DESIGN

(Common to IT and CSE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) If $1010_2 + 10_2 = X_{10}$, then X is -----

(b) Write the first 9 decimal digits in base 3.

(c) What is meant by don't care condition?

(d) Why AND and OR are not universal gates? Give the reason.

(e) Write the truth table of half subtractor.

(f) Implement AND gate using only two input NOR gates.

(g) Write the truth table of clocked T-Flip flop.

(h) Where the ripple counter is used?

(i) What is the function of EAROM?

(j) Mention few applications of PAL.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT - I

2 (a) Obtain the truth table for the function F = xy + xy' + y'z

(b) Prove that the sum of all minterms of a Boolean function for three variables is 1.

OR

3 (a) Show that the dual of the exclusive-OR is equal to its complement

(b) Convert the decimal number 1973 to base 3, base 5 and base 7.

UNIT - II

4 Simplify the following Boolean expressions using K-map and implement them using NAND gates:
F(W, X, Y, Z) = XZ + WXY + WXY + WYZ + WYZ.

OR

5 Simplify the following expression using tabulation method:
F(A, B, C, D, E) = ∑ (4, 6, 7, 9, 11, 12, 13, 14, 15, 20, 22, 25, 27, 28, 30) + d(1, 5, 29, 31).

UNIT - III

6 (a) How full adder is different from full subtractor? Explain.

(b) Draw and explain various implementations of full adder.

OR

7 (a) What is the function of magnitude comparator? Explain with an example.

(b) Design a combinational circuit with four input lines that represent a decimal digit in BCD and four output lines that generate the 9's complement of the input digit.

UNIT - IV

8 (a) Draw the block diagram of sequential circuit. Explain.

(b) What is state assignment? Explain with a suitable example.

OR

9 (a) Draw the basic flip flop circuit with NOR gates. Explain its operation.

(b) Explain about 3-bit binary counter with a suitable logic diagram.

UNIT - V

10 (a) Compare PAL and PLA with respect to various performance features.

(b) Explain about TTL family.

OR

11 (a) Explain about memory decoding error detection and correction.

(b) What is the importance of ECL family? Explain.

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