

**R13**

Code No: 114DN  
JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year II Semester Examinations, May - 2016

**PULSE AND DIGITAL CIRCUITS**

(Common to ECE, ETM)

Time: 3 Hours

Max. Marks: 75

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 25 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit.

Each question carries 10 marks and may have a, b, c as sub questions.

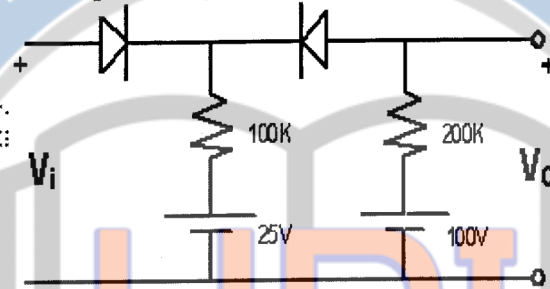
**PART - A (25 Marks)**

- 1.a) Why does resistive attenuator need to be compensated. [2]
- b) Derive an expression for the output of a high-pass circuit excited by a ramp input. [3]
- c) Draw the basic circuit diagram of negative peak clamper circuit. [2]
- d) Explain the working of an emitter coupled clipper. [3]
- e) Explain the effect of pedestal in gate circuit. [2]
- f) Explain the variation of saturation parameters of transistor with temperature? [3]
- g) Define UTP and LTP. [2]
- h) Write the difference between current time base generator and voltage time base generators. [3]
- i) Draw the diagram of OR gate using diodes. [2]
- j) Explain the principle of synchronization. [3]

**PART - B (50 Marks)**

- 2.a) A symmetrical square wave whose peak-to-peak amplitude is 8V and whose average value is zero is applied to an RC integrating circuit. The time constant is equal to half -period of the square wave. Find the peak to peak value of the output amplitude.
  - b) Explain the working of high-pass RC circuit as a differentiator. [5+5]
- OR**
- 3.a) Derive the expression for rise time of integrating circuit and prove that it is proportional to time constant and inversely proportional to upper 3 dB frequency.
  - b) Draw the response of the circuit for step input critically damped and over damped cases for a fixed value of R and C. [5+5]

- 4.a) For the circuit shown in figure, an input voltage  $V_i$  linearly varies from 0 to 120V is applied. Sketch the output voltage  $V_o$  to the same time scale. (Assume ideal diodes).



- b) State and prove the clamping circuit theorem. [5+5]

OR

- 5.a) Classify different types of clipper circuits. Give their circuits and explain their operation with the aid of transfer characteristics.

- b) Draw the basic circuit diagram of positive peak clamper circuit and explain its operation. [7+3]

- 6.a) Write a short note on switching times of a transistor.

- b) With the neat circuit diagram, explain the operation of unidirectional sampling gate for multiple inputs. [5+5]

OR

- 7.a) Discuss in detail about breakdown voltages of a transistor.

- b) Illustrate the errors encountered in series sampling and what is the design procedure to minimize these errors? [5+5]

- 8.a) With the help of neat circuit diagram and waveform, explain the principle of operation of collector coupled monostable multivibrator.

- b) Explain how the deviation from linearity is expressed in terms of errors. [6+4]

OR

- 9.a) With the help of a neat circuit diagram and waveforms, explain the working of a transistor bootstrap time base generator.

- b) What is hysteresis? Explain how hysteresis can be eliminated in a Schmitt trigger? [6+4]

- 10.a) Explain working of monostable relaxation device as a divider.

- b) Why totem pole is used in DTL? Draw the circuit diagram and explain a DTL NAND gate with this. [5+5]

OR

- 11.a) What is phase jitter? How to reduce it in frequency division?

- b) Draw and explain a diode AND circuit for negative logic and how it works. And how an OR circuit acts as a buffer circuit? [5+5]

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