

**II B. Tech II Semester Supplementary Examinations, Nov/Dec-2016**  
**SWITCHING THEORY AND LOGIC DESIGN**  
 (Com. to EEE, ECE, ECC, EIE)

Time: 3 hours

Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)  
2. Answer **ALL** the questions in **Part-A**  
3. Answer any **THREE** Questions from **Part-B**

## PART-A

1. a) Convert  $(53.1575)_{10}$  to  $(x)_2$
- b) Realize the X-OR gates using NAND gates.
- c) Draw the diagram of subtractor using truth tables.
- d) Explain the techniques used to eliminate the racing conditions in JK flip flops.
- e) Implement the Boolean functions with a PLA  $F(A,B,C) = \sum(0,5,6,7)$
- f) Draw the diagram of three bit shift register with waveforms.  $(3M+3M+4M+4M+4M+4M)$

## **PART-B**

2. a) What is the difference between canonical form and standard form? Explain.  
b) Solve the following
  - i)  $(27.125)_{10} = ( \quad )_8$
  - ii)  $(10.6875)_{10} = ( \quad )_2$
  - iii)  $(237.75)_8 = ( \quad )_{10}$(7M+9M)
3. a) Minimize the criterion the following using K-map.  
 $f(A,B,C,D) = \sum_m (0,1,2,3,5,6,7,8,9,10,11,13)$   
b) Minimize the following expression using K-map and realize using NOR gates.  
 $f = \prod M (1, 2, 3, 8, 9, 10, 11, 15)$ (8M+8M)
4. a) Design and draw a full adder which will use two half adders.  
b) Design Binary to Gray converter.(8M+8M)
5. a) Design a combinational circuit using PAL for the following function  
 $y(A,B,C,D) = \sum (0,2,3,4,5,6,7,8,10,11,15)$   
b) Clearly differentiate between Programmable Logic Array and Programmable Array Logic with examples.(8M+8M)
6. a) Design a mod-10 Ripple counter using T flip flops and explain its operation.  
b) What are the different types of registers? Explain the Serial Input Parallel Output shift register.(8M+8M)
7. a) Explain about sequential circuits, state table and state diagram.  
b) Explain the procedure of Mealy to Moore conversion.(8M+8M)

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