Subject Code: H6804/R13

M. Tech –II Semester Regular/ Supply Examinations, October, 2015

DESIGN FOR TESTABILITY

(Common to VLSI & ES, ES & VLSI, VLSID & ES, ES & VLSID, VLSI, VLSID, VLSISD and VLSI&ME,)

Time: 3 Hours **Max Marks: 60**

Answer any FIVE questions

All questions carry EQUAL marks

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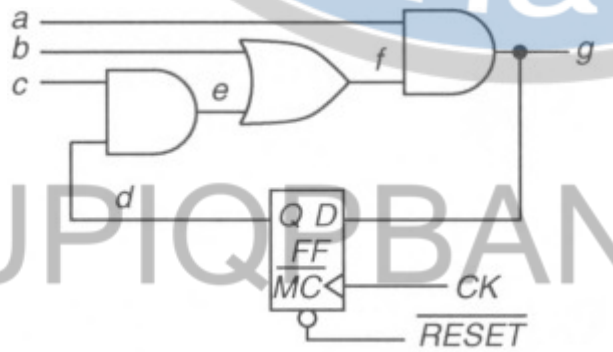
1. a) Define Defect? List out the different types of defects in VLSI chips?
   b) Discuss the different levels of fault models?

2. a) For a 2-input CMOS NAND circuit
   Find a two pattern test for each single transistor stuck-open fault
   For each stuck-at fault of the NAND gate, find an equivalent transistor fault.
   b) Illustrate the single stuck-at faults of combinational circuits with example?

3. a) Explain Transport Delays and Inertial delays in detail.
   b) Explain what action an event-driven true-value simulator will take when it evaluates a zero-delay gate.

4. a) What are the main differences between sequential SCOAP measures from the combinational measures. Explain with example.
   b) Compute the combinational and sequential SCOAP testability measures including CK and the synchronous RESET for the circuit shown below



5. a) Design an economical static CMOS two-to-one multiplexer.
   b) Explain the terms
      (i) Scan-Hold flip flop (SHFF)
      (ii) Random-Access Scan (RAS)

6. a) Draw the block diagram for a BIST implementation using BIBO and explain the test procedure.
   b) Explain the counter test technique for RAM BIST.

7. a) Describe the various JTAG TAP controller test instructions?
   b) Draw the TAP controller state diagram and timing diagrams?

8. a) Write a short note on Boundary scan description language?
   b) What is STUMPS? Explain how it is used for test-per-scan testing system?

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