Subject Code: H6809/R13

M. Tech –II Semester Regular/ Supply Examinations, October, 2015

LOW POWER VLSI DESIGN

(Common to VLSI&ES, ES&VLSI, VLSID&ES, ES& VLSID, VLSI, VLSID, VLSISD and VLSI&ME)

Time: 3 Hours **Max Marks: 60**

Answer any FIVE questions

All questions carry EQUAL marks

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1. (a) Write about sources of leakage power with neat diagram.
   (b) Write about Drain Induced Barrier Lowering of NMOS transistor.

2. (a) Write the advantages of Voltage scaling.
   (b) Write about pipe lining and parallel processing

3. (a) Realize CMOS logic for 1 bit full adder.
   (b) Write the drawbacks of ripple carry adder.

4. (a) What are the building blocks are needed for binary array multiplier and explain
   (b) Construct Baugh-Wooley Multiplier and explain its operation

5. (a) Design a 8X3 ROM and explain its operation.
   (b) Compare SRAM and DRAM memories.

6. (a) Design a carry-out circuit of 4 bit carry look ahead adder
   (b) Write the advantages and disadvantages of MTCMOS circuits.

7. (a) Explain the necessity of two-dimensional decoding mechanism in memories.
   (b) List out the sources of power dissipation in VLSI circuits and explain any two in detail.

8. (a) Write the drawbacks of carry look ahead adder.
   (b) Draw MOS transistor memory cell in ROM and explain the operation.

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