Code No: **RT42044C** **R13** **Set No. 1**

IV B.Tech II Semester Supplementary Examinations, July/August- 2017

LOW POWER VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B

*****

PART–A ***(22 Marks)***

1. a) Discuss about DIBL [3]
   b) Classify the types of multiplier architectures. [3]
   c) What is SPICE? [3]
   d) Realize CMOS logic for 1 bit full adder. [4]
   e) Write the advantages and disadvantages of MTCMOS circuits. [4]
   f) Draw the structure of a six transistor CMOS memory cell. [4]

PART–B ***(3x16 = 48 Marks)***

2. a) Discuss the need of low power VLSI design. [8]
   b) What are different types of power dissipation in CMOS circuits and discuss any three methods in detail. [8]

3. a) Explain the basic concepts of supply voltage scaling. [6]
   b) Briefly discuss about pipelining and parallel processing approaches with suitable examples. [10]

4. Write a notes on
   (i) static state power
   (ii) gate level capacitance estimation [6+10]

5. Discuss about an 8 bit architecture of CSA and explain with an example. [16]

6. a) What are the building blocks are needed for binary array multiplier and explain [8]
   b) Construct Baugh-Wooley Multiplier and explain its operation [8]

7. a) In what way the DRAMs differ from SRAMs? [4]
   b) Explain the read and write operations for a one-transistor transistor DRAM cell [12]