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06EC63

Sixth Semester B.E. Degree Examination, Dec.2013/Jan.2014
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Briefly explain the ADC specifications. **(06 Marks)**

b. Draw the waveforms of sample and hold, track and hold and show the typical errors associated with S/H in hold mode and sample mode with reasons. **(08 Marks)**

c. A digitally programmable signal generator uses a 14 bit DAC, with a 10V reference to generate a DC output voltage. What is the smallest incremental change at the output that can occur? What is the DAC's fullscale value? What is its accuracy? **(06 Marks)**

2 a. Design a 3 bit voltage mode DAC and determine the output voltage for each of the eight input codes, label each node voltage for each input. Assume that R = 1 KΩ and that $R_2 = R_1 = 10$ KΩ and $V_{REF} = 5V$. **(10 Marks)**

b. Briefly explain the architecture and working of cyclic DAC and show the value of the output voltage at the end of each cycle for a 6 bit cyclic DAC with an input value of 110101. Assume $V_{REF} = 5V$. **(10 Marks)**

3 a. Explain with a neat block diagram, dual slope integrated ADC and disucss the accuracy issues related to it. **(08 Marks)**

b. Explain with neat block diagram the working of 4 bit, two step flash ADC, make a table listing the MSB's, V_1, V_2, V_3 and LSB's for $V_{in} = 9V$ and 2V. Assume $V_{REF} = 16V$. **(08 Marks)**

c. For a charge scaling DAC, obtain the expression for $|INL|_{max}$ and $|DNL|_{max}$. **(04 Marks)**

4 a. Define nonlinear analog circuits with an example. **(02 Marks)**

b. Draw the basic block of comparator and explain pre-amplification and decision circuits of comparator. Draw their CMOS circuit. **(10 Marks)**

c. Explain the concept of analog multiplier. With relevant diagram, explain multiplier using squaring circuits. **(08 Marks)**

PART – B

5 a. Define SNR, effective number of bits and clock jitter in mixed signal circuits qualitatively. **(06 Marks)**

b. Explain the accumulate and dump circuit used for decimation in ADC. Draw the frequency response of the circuit for various values of K. **(08 Marks)**

c. Briefly explain the principle of frequency sampling filter. **(06 Marks)**

6 a. Define polycide, silicide, salicide and conductivity modulation. **(08 Marks)**

b. Explain true signal phase clocking (TSPC). Using TSPC, explain the delay element. **(08 Marks)**

c. Bring out the difference between normal CMOS process flow and submicron CMOS process flow. **(04 Marks)**

7 a. Draw the arrangement for 4 bit pipelined adder and full adder bit implemented using dynamic logic with brief explanation. **(06 Marks)**

b. Why do we need a boot strapped clock driver? With circuit explain its operation. **(08 Marks)**

c. Define MOSFET transition frequency and show how f_T is determined. **(06 Marks)**

8 a. Explain the limitation of inverter at the output of op-amp, with the help of its transfer curve. How is it overcome? **(06 Marks)**

b. Describe a mixed signal op-amp topology. **(08 Marks)**

c. Draw the schematic of a fully differential op-amp and also mixed signal op-amp building block with brief explanation. **(06 Marks)**

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06EC63

Sixth Semester B.E. Degree Examination, June/July 2013
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: *Answer FIVE full questions, selecting at least TWO questions from each part.*

PART – A

1 a. Explain about DAC (digital to analog converter) specifications. **(10 Marks)**

b. Find the resolution for a DAC if the output (o/p) voltage is desired to change in 1mV increments with $V_{ref} = 5V$. **(04 Marks)**

c. Using the Fig.Q.1(c), calculate the differential nonlinearity (DNL) of the 3-bit ADC. Assume that $V_{ref} = 5V$. Draw the quantization error (Q_e), in units of LρBs. **(06 Marks)**

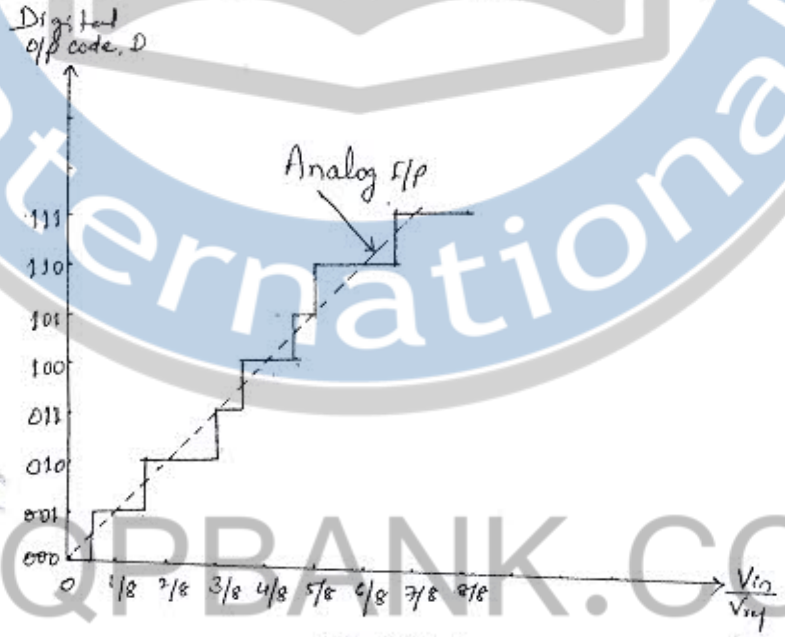

Fig.Q.1(c)

Transfer curve for a non-ideal 3-bit ADC.

2 a. Design a 3-bit resistor string ladder using a binary switch array. Assume that $V_{ref} = 5V$ and the maximum power dissipation of the converter is to be 5mW. Determine the value of the analog voltage for each of the possible digital I/P (input) codes. **(08 Marks)**

b. Which method is used to reduce the size of the capacitors in charge scaling DACs, explain with an example? **(08 Marks)**

c. Explain pipeline DAC with an example. **(04 Marks)**

3 a. Design a 3-bit flash ADC (analog to digital converter), listing the values of the voltages at each resistor tap, and draw the transfer curve (TC) for $V_{in} = 0$ to 5V. Assume $V_{ref} = 5V$. Construct a table listing the values of the thermometer code and the o/p of the decoder for $V_{in} = 1.5, 3, 4.5V$. **(10 Marks)**

b. Perform the operation of a 3-bit successive approximation ADC with the help of block diagram for $V_{ref} = 8V$. Make a table that consists of $D_2D_1D_0$, $B_2B_1B_0$, V_{out} (the o/p from the DAC) and the comparator output (V_{comp}) for $V_{in} = 5.5V$. **(10 Marks)**

4 a. Draw the block diagram of a voltage comparator. Explain in detail all the three stages of block diagram. **(10 Marks)**

b. Draw the circuit diagram of analog CMOS multiplier employing a multiplying quad with biasing arrangements. Write its voltage and current equations. **(10 Marks)**

PART – B

5 a. Determine the effective number of bits for an ADC with $V_{ref+} = 1.5V$, $V_{ref-} = 0$ and a measured $V_{Qe,RMS}$ of 2mV. **(06 Marks)**

b. Explain the accumulate and dump circuit used for decimation and averaging. Give the transfer function for the same. **(08 Marks)**

c. Explain the implementation of BPF (bandpass filter) using a comb filter and digital resonator. **(06 Marks)**

6 a. Explain CMOS process flow with neat sketches. **(12 Marks)**

b. Draw and explain n and p MOSFET switch and bidirectional nMOS switch to determine the resistance. **(08 Marks)**

7 a. Explain the delay element using True-single-phase clocking (TSPC) circuit and draw timing diagrams. **(10 Marks)**

b. Explain a 4-bit pipelined adder with the help of diagram. **(05 Marks)**

c. Draw the circuit diagram used to determine small-signal transconductance (gm) and the MOSFETs transition frequency (f_T). **(05 Marks)**

8 a. Explain the limitations of inverter at the o/p of op-amp, with the help of its transfer curve (TC). How it is overcome? **(08 Marks)**

b. Explain about some trade-offs in the design of mixed signal op-amp. **(06 Marks)**

c. Calculate the slew rate of the op-amp whose differential amplifier source 5μA current to charge the o/p MOSFETs whose widths $W_p = 400$ μm, $W_n = 200$ μm and $L = 2$μm at 0-15 μm technology. Assume $t_{ox} = 0.004$μm. **(06 Marks)**

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Sixth Semester B.E. Degree Examination, December 2012
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. With a neat diagram, explain the mixed signal layout strategy. **(07 Marks)**
b. Explain the different specifications of DAC. **(07 Marks)**
c. With a neat sketch, explain the typical errors associated with sample and hold circuit. **(06 Marks)**

2 a. With a neat diagram, explain the working of 3 bit pipeline DAC. **(07 Marks)**
b. With a neat circuit diagram, explain the working of R-2R ladder type DAC architecture. **(07 Marks)**
c. Determine the effective number of bits for a resistor string DAC which is assumed to be limited by the INL. The resistors are passive poly resistors with a known relative matching of 1% and V_{ref} = 5V. **(06 Marks)**

3 a. With the help of block diagram, explain the flash type ADC. **(07 Marks)**
b. With a neat block diagram, explain the working of successive approximation ADC. **(07 Marks)**
c. For an 8 bit single slope ADC with V_{ref} = 5V and clock frequency of 2 MHz, calculate the conversion time for an input of 2V. Also calculate the sampling frequency. **(06 Marks)**

4 a. With a neat block diagram, explain the working of voltage comparator. Also draw the schematic of pre-amplification stage of comparator. **(10 Marks)**
b. With a neat circuit diagram, explain the working of CMOS analog multiplier. Also explain the biasing of the multiplying quad. **(10 Marks)**

PART – B

5 a. With the help of block diagram explain the operation of an accumulate and dump circuit used for decimation and averaging. **(08 Marks)**
b. Explain the principle of interpolation and decimation. **(08 Marks)**
c. Determine the effective number of bits required for an ADC with a SNR of 50db. **(04 Marks)**

6 a. With neat sketches described the CMOS process. **(10 Marks)**
b. With neat CV curves explain natural MOSFET capacitor and floating MOS capacitor. **(10 Marks)**

7 a. With a neat circuit schematic, explain the working of a fulladder implemented using dynamic logic. **(07 Marks)**
b. Explain the simple delay element using clocked CMOS logic. **(07 Marks)**
c. Explain the design steps involved in analog circuit design. **(06 Marks)**

8 a. With a neat circuit schematic, explain the design of mixed signal op-amp. **(14 Marks)**
b. Explain fully differential op-amp. **(06 Marks)**

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06EC63

Sixth Semester B.E. Degree Examination, June 2012
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Determine the number of quantization levels needed if one wanted to make a digital thermometer that is capable of measuring temperature within 0.1°C accuracy over the range –50°C to 150°C. What is the resolution of ADC? **(04 Marks)**

b. Calculate DNL for a 3 bit ADC for the transfer curve shown in Fig.Q1(b). Assume V_{ref}= 5V. Draw the quantization error Q_e in units of LSB. **(06 Marks)**

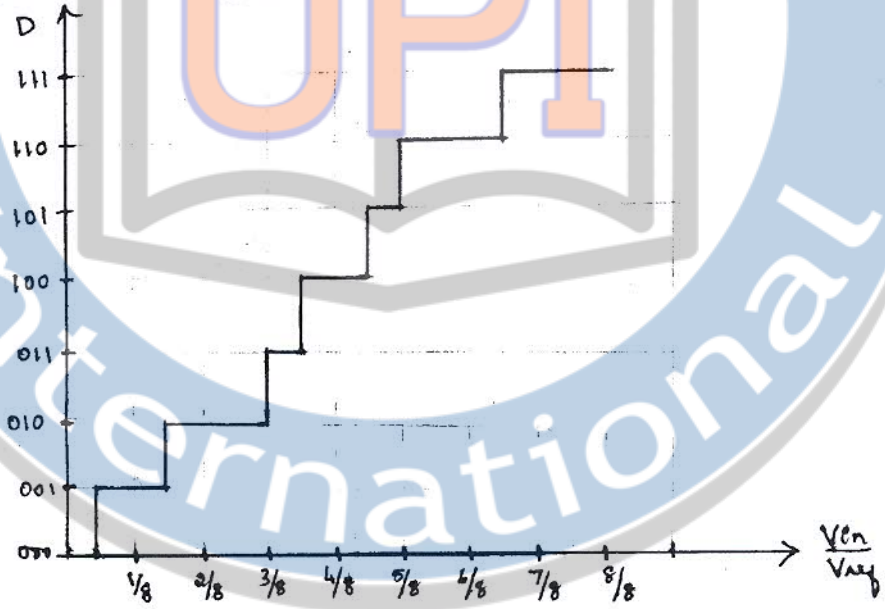

Fig.Q1(b)

c. With a neat diagram, explain the mixed signal layout issues in detail. **(10 Marks)**

2 a. Plot the transfer curve of a 3-bit R-2R DAC, if all R_s = 1.1 kΩ and $2R_s$ = 2 kΩ. What is the max INL for the converter? Assume all of the switch to be ideal and V_{ref} = 5 V. **(12 Marks)**

b. Design a 3 bit pipeline DAC and explain its operation. Also find the output voltage for a 3-bit pipeline DAC for 3 cases D_A = 101, D_B = 010, D_C = 011. Show that the conversion time to perform all three conversions is 5 clock cycles using pipeline approach. Assume V_{ref} = 5 V. **(08 Marks)**

3 a. With a neat diagram, explain the operation of a parallel feed through ADC along with its advantages and disadvantages. **(08 Marks)**

b. Design a 3 bit pipeline ADC. Analyse the conversion process by making a table for D_2, D_1, D_0, V_2, V_1 for V_{in} = 2V, 3V, 4.5V. Assume V_{ref} = 5V. Let V_3 be residue of 1st stage and V_2 be residue of 2nd stage. **(06 Marks)**

c. Explain the operation of a single slope ADC, with a neat diagram. **(06 Marks)**

4 a. Draw the block diagram of a high performance comparator and hence explain the operation of a decision circuit and obtain an expression for switching point. **(10 Marks)**

b. Explain the operation of a CMOS quad multiplier and hence obtain an expression for the multiplier output voltage. **(10 Marks)**

PART – B

5 a. Develop an expression for the effective number of bits in terms of measured SNR if the input sinewave has a peak amplitude of 40% of ($V_{ref+} - V_{ref-}$). **(06 Marks)**

b. Explain dump and interpolate circuit used for interpolation and reverse averaging. **(08 Marks)**

c. What is the magnitude response of $(1 - z^{-1})^3$. Sketch a block diagram implementation of the filter. **(06 Marks)**

6 a. Explain the sub-mirror CMOS process flow with a neat diagram. **(12 Marks)**

b. Estimate the size of Metal1 only to obtain the capacitance of 1 pF for the capacitor layout shown in Fig.Q6(b). Also estimate the bottom parasitic capacitance. **(04 Marks)**

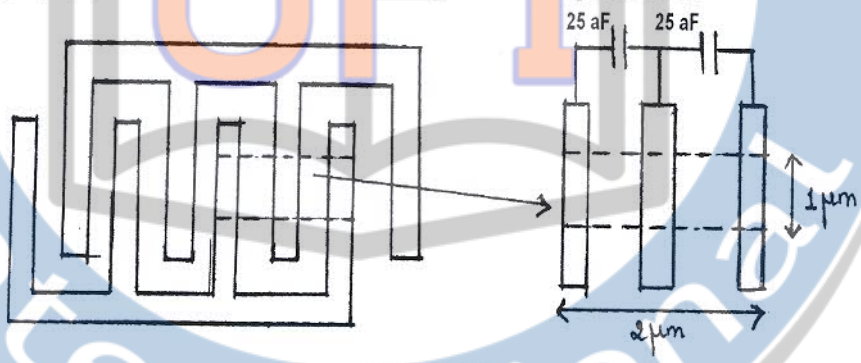

Fig.Q6(b)

c. Explain the fabrication of resistor using n-well. **(04 Marks)**

7 a. Explain the operation of D-Flip flop using TSPC logic and clocked CMOS logic with a neat diagram. **(08 Marks)**

b. Write the design equation for full adder. Using the equation, design full adder using dynamic logic. **(08 Marks)**

c. For the circuit shown in Fig.Q7(c), estimate the delay time. **(04 Marks)**

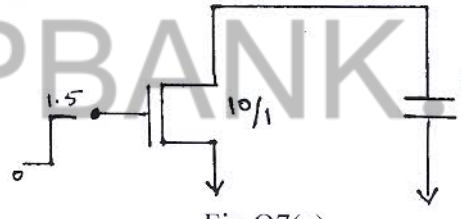

Fig.Q7(c)

8 a. Show that the floating current source will not load or decrease the resistance seen by cascade structure. **(08 Marks)**

b. Implement high speed, low power differential output op-amp and explain the operation. **(12 Marks)**

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06EC63

Sixth Semester B.E. Degree Examination, December 2011
Analog Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define DNL, INL, offset error, gain error. **(04 Marks)**

b. Explain the issues involved in mixed signal layout. **(10 Marks)**

c. Explain the working of a simple sample and hold circuit with the help of a circuit diagram. Explain the typical errors associated with the S/H circuit. **(06 Marks)**

2 a. With a neat block diagram, explain the working of a 3 bit pipelined DAC. List the advantages of the pipelined DAC over cyclic DAC. **(07 Marks)**

b. For a 3 bit pipelined DAC, find the outputs for inputs 001, 110 and 101 $V_{Ref} = 5V$. List the intermediate values with respect to clock cycles. **(08 Marks)**

c. Design a 3 bit DAC, using a binary switch array with $V_{Ref} = 5V$, power dissipation 5mW. Find the output for D = 011. **(05 Marks)**

3 a. For a 4 bit and 8 bit pipelined ADC if $V_{Ref} = 5V$ and $V_{in} = 2V$, find the digital output. Convert it back to the analog value. Comment on the result regarding the resolution of the converter. **(08 Marks)**

b. How would the design of the resistor string change for a 3 bit flash ADC, for the quantization error to be centered about '0' LSB? **(02 Marks)**

c. With a neat block diagram, explain the working of a dual slope integrating ADC. **(10 Marks)**

4 a. For a successive approximation ADC if $V_{in} = 2.49V$, what will be the output? If the comparator makes a mistake in the MSB, what will be the final output? $V_{Ref} = 5V$ N = 4. **(06 Marks)**

b. For an 8 bit dual slope ADC with $V_{Ref} = 5V$ and clock frequency 1MHz, what is the minimum and maximum conversion time? If $V_{in} = 2.5V$, what will be total conversion time? **(04 Marks)**

c. Explain the working of a comparator, with a block diagram. **(10 Marks)**

PART – B

5 a. Explain SNR, spurious free dynamic range, ENOB, SNDR. **(08 Marks)**

b. Develop an expression for ENOB in terms of the SNR measured, if the input sinewave has a peak to peak amplitude of 40% of $V_{Ref+} - V_{Ref-}$. **(04 Marks)**

c. Bring out the principle of interpolation and decimation. **(08 Marks)**

6 a. With a neat block diagram, explain the accumulator and dump circuit. Plot the general frequency response of an averaging filter. **(10 Marks)**

b. Sketch the block level circuit diagram of a fs/4 digital resonator after deriving the transfer function. **(05 Marks)**

c. Discuss the advantages and disadvantages of cascading averaging circuits to increase filter attenuation. **(05 Marks)**

7 a. Describe the CMOS process flow with neat sketches. **(10 Marks)**

b. Explain how MOSFET behaves as a capacitor. Also explain the floating MOS capacitor. **(06 Marks)**

c. Explain the simple delay element, using the pass transistors and CMOS inverters. **(04 Marks)**

8 a. Draw the arrangement for a 4 bit pipelined adder and full adder bit implemented, using the dynamic logic. **(08 Marks)**

b. Explain the limitation of inverter at the output of op-amp with the help of its transfer curve. How is it overcome? **(06 Marks)**

c. Estimate the high to low and low to high delays in **(06 Marks)**

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06EC63

Sixth Semester B.E. Degree Examination, June/July 2011
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: *1. Answer FIVE full questions selecting at least TWO questions from each part.*
2. Missing data may be suitably assumed.

PART – A

1 a. Explain the characteristics of a sample and hold circuit used in converting analog signals to digital signals. **(06 Marks)**

b. Determine the maximum DNL (in LSBs) for a 3-bit DAC which has the following characteristics. Does the DAC have 3-bit accuracy? If not, what is the resolution of the DAC having this characteristic? **(05 Marks)**

Digital Input	000	001	010	011	100	101	110	111
Voltage output in V	0	0.625	1.5625	2.0	2.5	3.125	3.4375	4.375

c. Explain in detail the issues in mixed signal layouts with reference to:
i) floor planning ii) power supply and grounding issues iii) shielding. **(09 Marks)**

2 a. Explain charge scaling DACs and layout considerations for a binary weighted capacitor array. **(08 Marks)**

b. A 3-bit resistor string DAC was designed with a desired resister of 500 Ω. After fabrication, mismatch caused the actual value of the resistors to be,
$R_1 = 500\Omega$, $R_2 = 480\Omega$, $R_3 = 470\Omega$, $R_4 = 520\Omega$, $R_5 = 510\Omega$, $R_6 = 490\Omega$, $R_7 = 530\Omega$ and $R_8 = 500\Omega$.
Determine the maximum INL and DNL for the DAC assuming $V_{ref} = 5$ V. **(06 Marks)**

c. For a binary weighted current steering DAC, obtain the expression for $|INL|_{max}$ and $|DNL|_{max}$ **(06 Marks)**

3 a. With a neat block diagram, explain the successive approximation ADC. Draw the relevant binary search waveform for a 3-bit with D = 101. **(08 Marks)**

b. Design a 3-bit flash ADC with its quantization error centered about zero LSBs. Determine the worst-case DNL and INL, if resistor matching is known to be 5%. Assume that $V_{ref} = 5$V. **(06 Marks)**

c. Explain with a block diagram, dual slope integrated ADC. **(06 Marks)**

4 a. With a relevant diagram using MOSFETs, explain the 3-stages of a voltage comparator. **(12 Marks)**

b. Explain the concept of analog multiplier. With relevant diagram describe the warping of a CMOS multiplier that uses multiplying quad. **(08 Marks)**

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – B

5 a. Assuming rms quantization noise voltage to be $V_{LSB}/\sqrt{12}$. Show that averaging the outputs of a data converter will improve SNR. **(05 Marks)**

b. Explain the accumulate and dump circuit used for decimation in ADC. Draw the frequency response of the circuit for various values of K. **(10 Marks)**

c. Describe the bandpass filter implementation using a comb filter and a digital resonator. **(05 Marks)**

6 a. With a neat diagram, explain the CMOS process flow for sub – 0.35μm process. **(07 Marks)**

b. Describe the method of implementation of a floating MOS capacitor. **(06 Marks)**

c. Explain how a simple delay element can be realized using i) pass transistor and ii) clock CMOS logic. **(07 Marks)**

7 a. With a neat circuit, explain the working of a 4-bit pipelined adder. Draw the circuit used for implementing 1-bit full adder. **(10 Marks)**

b. Describe the implementation of a switch using NMOS and PMOS logic. **(06 Marks)**

c. Explain the procedures for selecting the channel length of a MOSFET, in analog circuit design. **(04 Marks)**

8 a. Explain the process of biasing a push-pull amplifier o/p stage with a floating current design. **(05 Marks)**

b. Describe the operation of differential amplifier that uses source follower level shifter for boosting OP-AMP gain. **(07 Marks)**

c. Describe a mixed signal OP-AMP topology. **(08 Marks)**

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b. Explain the working of

5 a. Give the Z domain rep response of the digital

b. If the input sinewave 20MHz, determine the circuit.

c. Develop an expression input sinewave has a p

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06EC63

Sixth Semester B.E. Degree Examination, May/June 2010
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the characteristics and typical errors associated with sample and hold circuit. **(10 Marks)**

b. Briefly explain the ADC specifications. **(05 Marks)**

c. Find the resolution of DAC, if the output voltage is desired to change in 1 mV increments while using a reference voltage of 4V. **(05 Marks)**

2 a. Explain qualitatively the architecture and working of charge scaling DACs. **(10 Marks)**

b. Design a 3-bit charge scaling DAC and find the value of output voltage for $D_2D_1D_0$ = 100 and 011. Assume V_{ref} = 5V, C = 0.5 PF. **(05 Marks)**

c. Briefly explain the architecture & working of a pipeline digital to analog coverter. **(05 Marks)**

3 a. Explain the architecture and working of a flash ADC. **(08 Marks)**

b. If a 10-bit flash ADC is designed, determine maximum offset voltage of comparators which will make INL less than ½ LSB. Assume that resister string is perfectly matched and V_{REF} = 4V. **(04 Marks)**

c. Briefly explain the block diagram of a 2-step flash ADC and its working. **(08 Marks)**

4 a. Explain qualitatively preamplification and decision circuits of a CMOS comparator unit. Draw their CMOS circuits. **(10 Marks)**

b. Explain the principle of an analog multiplier. **(05 Marks)**

c. Briefly explain CMOS analog multiplier with the help of a circuit diagram. **(05 Marks)**

PART – B

5 a. Define SNR, effective number of bits and clock jitter in mixed signal circuits qualitatively. **(08 Marks)**

b. Explain the principle of averaging to improve SNR, in mixed signal circuits. **(06 Marks)**

c. Briefly explain the role of decimating filters in ADCs. **(06 Marks)**

6 a. With a neat process flow diagram, explain submicron CMOS technology and bring out the differences as compared to CMOS technology. **(10 Marks)**

b. Explain how capacitor and resister elements are fabricated in submicron technology. **(07 Marks)**

c. Explain MOSFET as a switch. **(03 Marks)**

7 a. What are delay elements? Explain how they are realized using pass transistors, inverters and C^2MOS and TSPC circuits. **(10 Marks)**

b. Realize a 4-bit pipelined adder using latches and explain its operation. **(05 Marks)**

c. Implement full adder using dynamic logic and explain. **(05 Marks)**

8 a. Consider a small signal amplification of a floating current source shown in Fig.Q8(A). Assuming NMOS cascade o/p resistance is labeled R_{ncas} , what is the small signal resistance scan by test voltage V_{test}? **(10 Marks)**

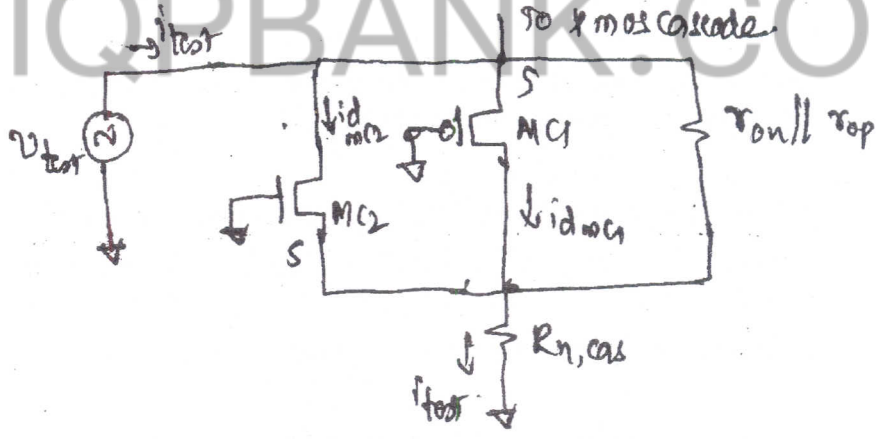

Fig.Q8(A)

b. Explain with the help of circuit diagrams, the technique of making the flow rate concern in the design of op amp. **(10 Marks)**

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06EC63

Sixth Semester B.E. Degree Examination, May/June 2010
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the characteristics and typical errors associated with sample and hold circuit. **(10 Marks)**

b. Briefly explain the ADC specifications. **(05 Marks)**

c. Find the resolution of DAC, if the output voltage is desired to change in 1 mV increments while using a reference voltage of 4V. **(05 Marks)**

2 a. Explain qualitatively the architecture and working of charge scaling DACs. **(10 Marks)**

b. Design a 3-bit charge scaling DAC and find the value of output voltage for $D_2D_1D_0$ = 100 and 011. Assume V_{ref} = 5V, C = 0.5 PF. **(05 Marks)**

c. Briefly explain the architecture & working of a pipeline digital to analog coverter. **(05 Marks)**

3 a. Explain the architecture and working of a flash ADC. **(08 Marks)**

b. If a 10-bit flash ADC is designed, determine maximum offset voltage of comparators which will make INL less than ½ LSB. Assume that resister string is perfectly matched and V_{REF} = 4V. **(04 Marks)**

c. Briefly explain the block diagram of a 2-step flash ADC and its working. **(08 Marks)**

4 a. Explain qualitatively preamplification and decision circuits of a CMOS comparator unit. Draw their CMOS circuits. **(10 Marks)**

b. Explain the principle of an analog multiplier. **(05 Marks)**

c. Briefly explain CMOS analog multiplier with the help of a circuit diagram. **(05 Marks)**

PART – B

5 a. Define SNR, effective number of bits and clock jitter in mixed signal circuits qualitatively. **(08 Marks)**

b. Explain the principle of averaging to improve SNR, in mixed signal circuits. **(06 Marks)**

c. Briefly explain the role of decimating filters in ADCs. **(06 Marks)**

6 a. With a neat process flow diagram, explain submicron CMOS technology and bring out the differences as compared to CMOS technology. **(10 Marks)**

b. Explain how capacitor and resister elements are fabricated in submicron technology. **(07 Marks)**

c. Explain MOSFET as a switch. **(03 Marks)**

7 a. What are delay elements? Explain how they are realized using pass transistors, inverters and C^2MOS and TSPC circuits. **(10 Marks)**

b. Realize a 4-bit pipelined adder using latches and explain its operation. **(05 Marks)**

c. Implement full adder using dynamic logic and explain. **(05 Marks)**

8 a. Consider a small signal amplification of a floating current source shown in Fig.Q8(A). Assuming NMOS cascade o/p resistance is labeled R_{ncas} , what is the small signal resistance scan by test voltage V_{test}? **(10 Marks)**

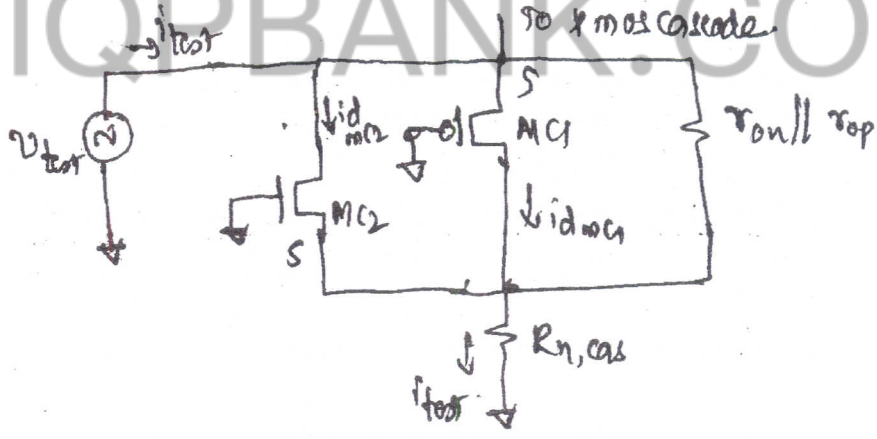

Fig.Q8(A)

b. Explain with the help of circuit diagrams, the technique of making the flow rate concern in the design of op amp. **(10 Marks)**

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06EC63

Sixth Semester BE Degree Examination, Dec.09-Jan.10
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions, selecting at least TWO questions from each part.*
2. Standard notations are used.
3. Missing data be suitably assumed.

PART – A

1 a. Define Resolution, INL, DNL and V_{FS} for a DAC. **(06 Marks)**

b. Find the maximum DNL and INL in LSBs of a 3 bit DAC which has the following characteristics. Check if it is monotonic. **(10 Marks)**

Digital input	000	001	010	011	100	101	110	111
Analog output	0 V	0.625 V	1.5625 V	2.0 V	2.5 V	3.125 V	3.4375 V	4.375 V

c. Find the maximum resolution of an ADC which can use the S/H circuit with maximum sampling error of 0.628 mV while maintaining a sampling error less than 1/2 LSB Vref = 5V. **(04 Marks)**

2 a. Discuss the issues involved in mixed signal circuit layout. **(10 Marks)**

b. Describe the simple resistor string DAC, problem associated with it and how is it overcome by use of a binary switch array. **(10 Marks)**

3 a. Describe the pipelined ADC with a neat diagram. **(08 Marks)**

b. For an 8 bit pipelined ADC, all the amplifiers had a gain of 2.1 v/v instead of 2v/v. If V_{in} = 3V and V_{ref} = 5V, what would be the resulting digital output, assuming other components are ideal. **(06 Marks)**

c. For a 4 bit successive approximation ADC with V_{ref} = 5V, V_{in} = 1V, find the output digital code. Assume a dual slope successive approximation ADC. For each clock cycle, give the output of the SAR, V_{aut} and the final output. **(06 Marks)**

4 a. Discuss the advantages and disadvantages of using a dual slope over a single slope ADC. **(06 Marks)**

b. Draw the CMOS analog multiplier and explain its working. **(07 Marks)**

c. Discuss transient response, propagation delay and minimum slewrate of a comparator. **(07 Marks)**

PART – B

5 a. Develop an expression for effective number of bits in terms of the measured SNR if the input wave has a peak amplitude of 30% of V_{ref}. **(07 Marks)**

b. With a neat block diagram, describe the accumlate and dump circuit for decimation and averaging. **(07 Marks)**

c. Sketch the block level circuit diagram for an fs/4 digital resonator. **(06 Marks)**

6 a. With relevant diagrams, describe the CMOS process flow, for devices with L_{min} <0.35 μm. **(10 Marks)**

b. Describe with a neat diagram, the conceptual layout and actual layout of an R-2R resistor string with minimum area and also discuss the problem of laying out metal over the resistive material. **(10 Marks)**

7 a. Sketch the implementation of a synchronous up/down counter and discuss its operation. **(07 Marks)**

b. Draw the 4 bit pipelined adder and describe how it operates. **(08 Marks)**

c. Draw the positive edge triggered delay using clocked CMOS logic. **(05 Marks)**

8 a. Illustrate how a pushpull output stage is biased with a floating current source. **(07 Marks)**

b. Infer that, to minimize the input referred noise, the gain of the first stage of the amplifier should be large in a cascade of amplifiers. **(06 Marks)**

c. Discuss circuit noise in an opamp. **(07 Marks)**

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06EC63

Sixth Semester BE Degree Examination, Dec.09-Jan.10
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions, selecting at least TWO questions from each part.*
2. Standard notations are used.
3. Missing data be suitably assumed.

PART – A

1 a. Define Resolution, INL, DNL and V_{FS} for a DAC. **(06 Marks)**

b. Find the maximum DNL and INL in LSBs of a 3 bit DAC which has the following characteristics. Check if it is monotonic. **(10 Marks)**

Digital input	000	001	010	011	100	101	110	111
Analog output	0 V	0.625 V	1.5625 V	2.0 V	2.5 V	3.125 V	3.4375 V	4.375 V

c. Find the maximum resolution of an ADC which can use the S/H circuit with maximum sampling error of 0.628 mV while maintaining a sampling error less than 1/2 LSB Vref = 5V. **(04 Marks)**

2 a. Discuss the issues involved in mixed signal circuit layout. **(10 Marks)**

b. Describe the simple resistor string DAC, problem associated with it and how is it overcome by use of a binary switch array. **(10 Marks)**

3 a. Describe the pipelined ADC with a neat diagram. **(08 Marks)**

b. For an 8 bit pipelined ADC, all the amplifiers had a gain of 2.1 v/v instead of 2v/v. If V_{in} = 3V and V_{ref} = 5V, what would be the resulting digital output, assuming other components are ideal. **(06 Marks)**

c. For a 4 bit successive approximation ADC with V_{ref} = 5V, V_{in} = 1V, find the output digital code. Assume a dual slope successive approximation ADC. For each clock cycle, give the output of the SAR, V_{aut} and the final output. **(06 Marks)**

4 a. Discuss the advantages and disadvantages of using a dual slope over a single slope ADC. **(06 Marks)**

b. Draw the CMOS analog multiplier and explain its working. **(07 Marks)**

c. Discuss transient response, propagation delay and minimum slewrate of a comparator. **(07 Marks)**

PART – B

5 a. Develop an expression for effective number of bits in terms of the measured SNR if the input wave has a peak amplitude of 30% of V_{ref}. **(07 Marks)**

b. With a neat block diagram, describe the accumlate and dump circuit for decimation and averaging. **(07 Marks)**

c. Sketch the block level circuit diagram for an fs/4 digital resonator. **(06 Marks)**

6 a. With relevant diagrams, describe the CMOS process flow, for devices with L_{min} <0.35 μm. **(10 Marks)**

b. Describe with a neat diagram, the conceptual layout and actual layout of an R-2R resistor string with minimum area and also discuss the problem of laying out metal over the resistive material. **(10 Marks)**

7 a. Sketch the implementation of a synchronous up/down counter and discuss its operation. **(07 Marks)**

b. Draw the 4 bit pipelined adder and describe how it operates. **(08 Marks)**

c. Draw the positive edge triggered delay using clocked CMOS logic. **(05 Marks)**

8 a. Illustrate how a pushpull output stage is biased with a floating current source. **(07 Marks)**

b. Infer that, to minimize the input referred noise, the gain of the first stage of the amplifier should be large in a cascade of amplifiers. **(06 Marks)**

c. Discuss circuit noise in an opamp. **(07 Marks)**

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06EC63

Sixth Semester B.E. Degree Examination, June-July 2009
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. State the reasons for the pedestal error, droop aperture error and sampling error. **(08 Marks)**

b. State and explain specifications of ADC. **(12 Marks)**

2 a. An 8 bit resistor string DAC was fabricated with a nominal resistor value of 1 kΩ. If the process was able to provide matching of resistors to within 1%, find maximum INL and DNL of the converter. Assume $V_{REF} = 5V$. **(06 Marks)**

b. Explain generic (unweighted) current steering DAC and discuss the related mismatch errors. **(08 Marks)**

c. Design a 4 bit charge scaling DAC using a split array. Assume that $V_{REF} = 5V$ and that C = 0.5 pF. Draw the equivalent circuit for D = 0001 and 0010 and determine the value of the output voltage. **(06 Marks)**

3 a. Explain the principle of single slope ADC and the problems associated with it. **(10 Marks)**

b. Draw the block diagram for 4 bit successive approximation ADC with $V_{REF} = 5V$. Explain the same. Trace the output at various stages for $V_{in} = 3.7V$. **(10 Marks)**

4 a. Explain the purpose of each stage of a voltage comparator. Also explain the working of 1st stage. **(10 Marks)**

b. Show that multiplying quad acts as multiplier when all the MOSFETs in the multiplying quad have the same threshold voltage. **(10 Marks)**

PART – B

5 a. Determine the ideal SNR of a 8 bit data converter with averaging of 20 outputs. **(04 Marks)**

b. Draw the circuit arrangement used for decimation and averaging and explain the same. Determine the transfer function of the same. **(10 Marks)**

c. Bring out the principle of interpolation. **(06 Marks)**

6 a. Describe CMOS process flow with neat sketches. **(10 Marks)**

b. Explain how MOSFET behaves as a capacitor. Also explain floating MOS capacitor. **(10 Marks)**

7 a. Estimate the high-to-low and low-to-high delays in the circuits shown in figure Q7 (a). **(08 Marks)**

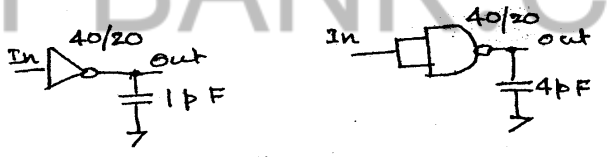

Fig. Q7 (a)

b. Draw the arrangement for 4 bit pipelined adder and full adder bit implemented using dynamic logic. **(06 Marks)**

c. Explain the working of simple delay element using pass transistor and CMOS inverter. **(06 Marks)**

8 a. Explain the limitations of inverter at the output of OPAMP, with the help of its transfer curve. How is it overcome? **(07 Marks)**

b. Consider the AC small signal simplification of floating current source as in figure Q8 (b). Assuming NMOS cascade output resistance is labeled R_{NCOS}, what is the small signal resistance as seen by the test voltage V_{test}? **(07 Marks)**

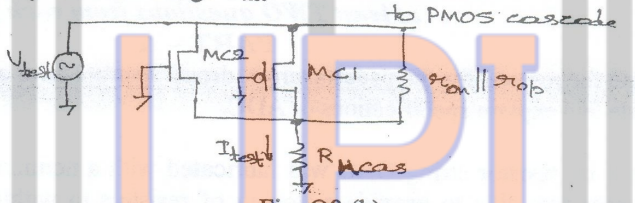

Fig. Q8 (b)

c. Determine time constant of OPAMP with unity gain frequency of 100 MHz. Assume that all the outputs is fed back to the input. Also determine the settling time for 0.1% settling accuracy. **(06 Marks)**

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06EC63

Sixth Semester B.E. Degree Examination, June-July 2009
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. State the reasons for the pedestal error, droop aperture error and sampling error. **(08 Marks)**

b. State and explain specifications of ADC. **(12 Marks)**

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b. Draw the block diagram for 4 bit successive approximation ADC with $V_{REF} = 5V$. Explain the same. Trace the output at various stages for $V_{in} = 3.7V$. **(10 Marks)**

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PART – B

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b. Draw the circuit arrangement used for decimation and averaging and explain the same. Determine the transfer function of the same. **(10 Marks)**

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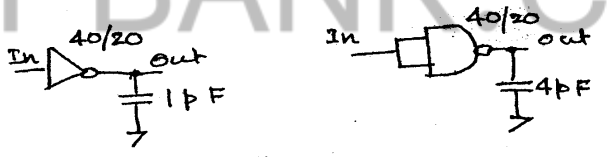

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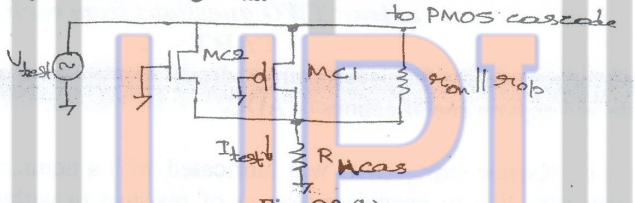

Fig. Q8 (b)

c. Determine time constant of OPAMP with unity gain frequency of 100 MHz. Assume that all the outputs is fed back to the input. Also determine the settling time for 0.1% settling accuracy. **(06 Marks)**

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