Code: 15A05402

R15

B.Tech III Year I Semester (R15) Regular Examinations November/December 2017

COMPUTER ORGANIZATION

(Electronics and Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Draw the single-bus structure.
(b) Make a comparisons between the multiprocessor and multicomputer.
(c) Represent decimal number 6027 in: (i) BCD. (ii) Excess-3
(d) Mention and describe the fast multiplication algorithm.
(e) Distinguish between the virtual memory and cache memory
(f) Write a short note on static RAM.
(g) How DMA Controller works?
(h) What is the importance of I/O interface?
(i) Write a short note on array processor.
(j) Define data hazard. List the three situations under which a data hazard can occur.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 With the help of neat diagram, explain the connections between the processor and main memory. Also explain the typical operating steps involving instruction fetch and execution.

OR

3 What is an Addressing mode? List and explain the various addressing modes with an example.

UNIT – II

4 Explain with examples, how the floating-point numbers are represented and used in digital arithmetic operations. Give an example.

OR

5 Give the organization of typical hardwired control unit and explain the functions performed by the various blocks.

UNIT – III

6 (a) A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.

(b) Draw and explain the organization of a memory chip.

OR

7 (a) A computer uses RAM chips of 1024 X 1 capacity.
(i) How many chips are needed, and should their address lines be connected to provide a memory capacity of 1024 bytes?
(ii) How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus.

(b) Give a brief note on secondary storage in detail.

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UNIT – IV

8 What is the problem with programmed I/O? Explain the alternate for it. Also using block diagram explain DMA data transfer.

OR

9 How are the I/O devices connected to CPU & Memory? What is an I/O interface? With a neat block diagram, explain three sections of I/O modules.

UNIT – V

10 (a) Draw and explain the structure of general purpose multicomputer.

(b) What are pipeline hazards? List and define various conflicts that might arise in a pipeline.

OR

11 (a) Draw and explain the working of 8 x 8 omega Switching network.

(b) With a neat diagram, explain Multiport memory organization.

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