Code: 15A04510

R15

B.Tech III Year I Semester (R15) Regular Examinations November/December 2017

DIGITAL CIRCUITS & SYSTEMS

(Electrical & Electronics Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Convert $(2468)_{10}$ to $(\ )_{16}$.

(b) Define prime implicant and essential prime implicants of a Boolean expression.

(c) List the applications of multiplexers.

(d) Design 2x4 decoder using NAND gates.

(e) Write the difference between counter and register.

(f) Draw and explain active low S-R latch.

(g) What is a PLD? What is the principal advantage of a PLD?

(h) Write the demerits of PROM.

(i) Define sequential circuits and active clock edge.

(j) Explain the use of algorithmic state machine.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) What is the difference between canonical form and standard form? Explain.

(b) Perform the subtraction using 1's complement and 2's complement methods.

(i) 11010 – 10000. (ii) 11010 – 1101.

OR

3 Find the complement of the following Boolean functions and reduce them to minimum number of literals.

(i) $(bc^1 + a^1d)(ab^1 + cd^1)$.

(ii) $(b^1d + a^1bc^1 + acd + a^1bc)$.

UNIT – II

4 (a) Reduce the following function using k-map technique.

$F(A, B, C, D) = \Pi(0,2,3,8,9,12,13,15)$.

(b) Minimize the expression using k-map.

$y = (A + B + C^1)(A + B + C)(A^1 + B^1 + C^1)(A^1 + B + C)(A + B + C)$

OR

5 Simply the following using tabulation method.

$y(w, x, y, z) = \Sigma\, m(1,2,3,5,9,12,14,15) + d(4,8,11)$

UNIT – III

6 (a) Design a type-D counter that goes through states 0, 2, 4, 6, 0……. The undesired states must always go to a 0 on the next clock pulse.

(b) Draw the schematic circuit of an edge-triggered JK flip flop using NAND gates and deduce its truth table.

OR

7 (a) Design and draw a full adder which will use two half adders.

(b) What are the different types of registers? Explain the serial input parallel output shift register.

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UNIT – IV

8 (a) Design a PAL for the following logical functions.
$Y_1 = AB + A^1CB^1,\ Y_2 = AB^1C + AB + AC^1,\ Y_3 = AB + BC + CA$

(b) Discuss how PROM, EPROM and EEPROM technologies differ from each other.

OR

9 (a) Implement the following multiple output functions using PROM.
$F_1 = \Sigma m(0, 1, 4, 7, 12, 14, 15)$
$F_2 = \Sigma m(1, 3, 6, 9, 12)$
$F_3 = \Sigma m(2, 3, 7, 8, 10)$
$F_4 = \Sigma m(1, 3, 5)$

(b) Implement $f(A, B, C, D) = \Sigma(0,1,4,5,6,7,9,10,12,13,15)$ using PLA and explain its procedure.

UNIT – V

10 Explain in detail the mealy state diagram with one example.

OR

11 (a) Draw a state diagram of a sequence detector which can detect 110.

(b) Explain the state machine capabilities and limitations in detail.

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