

B.Tech III Year I Semester (R15) Regular Examinations November/December 2017

DIGITAL SYSTEM DESIGN

(Electronics and Communication Engineering)

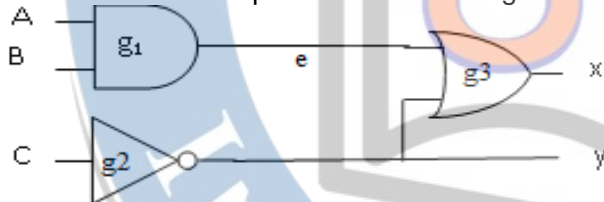
Time: 3 hours

Max. Marks: 70

PART – A

(Compulsory Question)

- 1 Answer the following: (10 X 02 = 20 Marks)
- Which is faster TTL or ECL? Which requires more power to operate?
 - State the characteristics of CMOS family.
 - Write the HDL data flow description of 4 bit adder.
 - Give the HDL description for the following circuit.



- Why the input variables to a PAL are buffered?
- Draw the circuit diagram for 2 to 1 line multiplexer.
- How many states are there in a 3 bit ring counter?
- Write any two applications of shift register.
- Apply gate level model to write a Verilog code for 4-to-2 Encoder.
- What is meant by latches?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

- 2 With suitable diagrams, explain the interfacing of low voltage CMOS logic with TTL logic family.

OR

- 3 Design a CMOS inverter and explain its operation. Comment on its characteristics such as FAN-in, Fan-out, power dissipation, and propagation delay and noise margin. Compare its advantages over other logic families.

UNIT – II

- Outline the function of test benches of VHDL.
- Explain the VHDL features for sequential logic design.

OR

- 5 Enumerate on the structural design elements and behavioral design elements of VHDL with suitable examples.

UNIT – III

- 6 Conclude that the carry look ahead adder is faster than a ripple carry Adder by using necessary equations.

OR

- 7 Implement the following Boolean function using $3 \times 4 \times 2$ PLA, $F_1(x, y, z) = \sum (0, 1, 3, 5)$ and $F_2(x, y, z) = \sum (3, 5, 7)$.

UNIT – IV

- 8 A sequential machine has one input line where 0's and 1's are being incident. The machine has to produce the output of '1' only when exactly two '0's are followed by '1' or exactly two '1's are followed by a '0'. Using any statement assignment in JK flip flop, synthesize the machine.

OR

- 9 Design and explain the working of 4 bit Johnson counter with neat logic diagram.

UNIT – V

- 10 Develop and test the dual parity encoder by writing VHDL program.

OR

- 11 Analyze the steps involved in the design of shift register using VHDL model.
