Code: 13A04509 **R13**

B.Tech III Year I Semester (R13) Supplementary Examinations November/December 2017

LINEAR & DIGITAL IC APPLICATIONS

(Electronics and Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) What is the need for frequency compensation in practical op-amps?
(b) List the desirable characteristics of an instrumentation amplifier.
(c) What is the need of an op-amp multivibrator?
(d) List the applications of IC555 timer in monostable mode of operation.
(e) Classify the bipolar logic family by operation and give examples for each category.
(f) List some of the differences between CMOS and TTL logic families.
(g) List out various steps in an HDL-based design flow.
(h) Draw a diagram of the circuit specified by the VHDL code fragment shown below.

```
architecture STR of STRAD is
componentXOR2
port(X, Y: in BIT; Z: out BIT);
end component;
component AND2
port(L, M: in BIT; N: out BIT);
end component;
begin
X1: XOR2 port map (A, B, SUM);
A1: AND2 port map (A, B, CARRY);
end STR;
```

(i) Write any two applications of shift registers.
(j) What is a PLD? Write the classification of PLDs.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

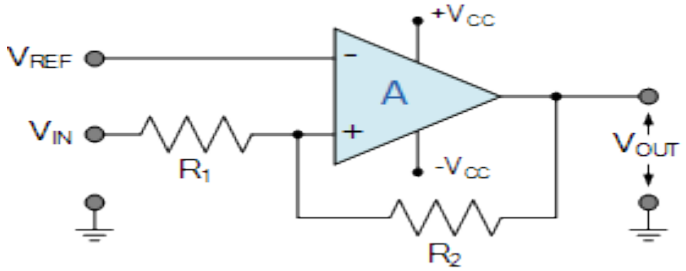
2 (a) Design an inverting amplifier with an input resistance of 2 kΩ, an output resistance of 100 Ω and an open-circuit voltage gain of −30.
(b) List out ideal OP-AMP characteristics.

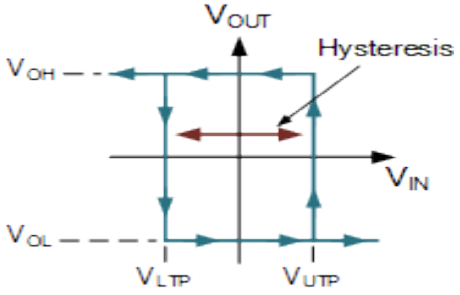
OR

3 (a) Design a modified differentiator which has a time constant of 10 ms and a pole frequency of 1 kHz. For a 1 V peak sine-wave input signal at 100 Hz, calculate the peak sine wave output voltage and the relative phase of the output voltage.
(b) What are the main features of IC 741 OP-AMP?

UNIT – II

4 An operational amplifier is to be used with positive feedback to produce a Schmitt trigger circuit. If resistor, R_1 = 10 kΩ and resistor, R_2 = 90 kΩ, what will be the values of the upper and lower switching points of the reference voltage and the width of the hysteresis if the op-amp is connected to a dual ±10 V power supply as shown in figure below.





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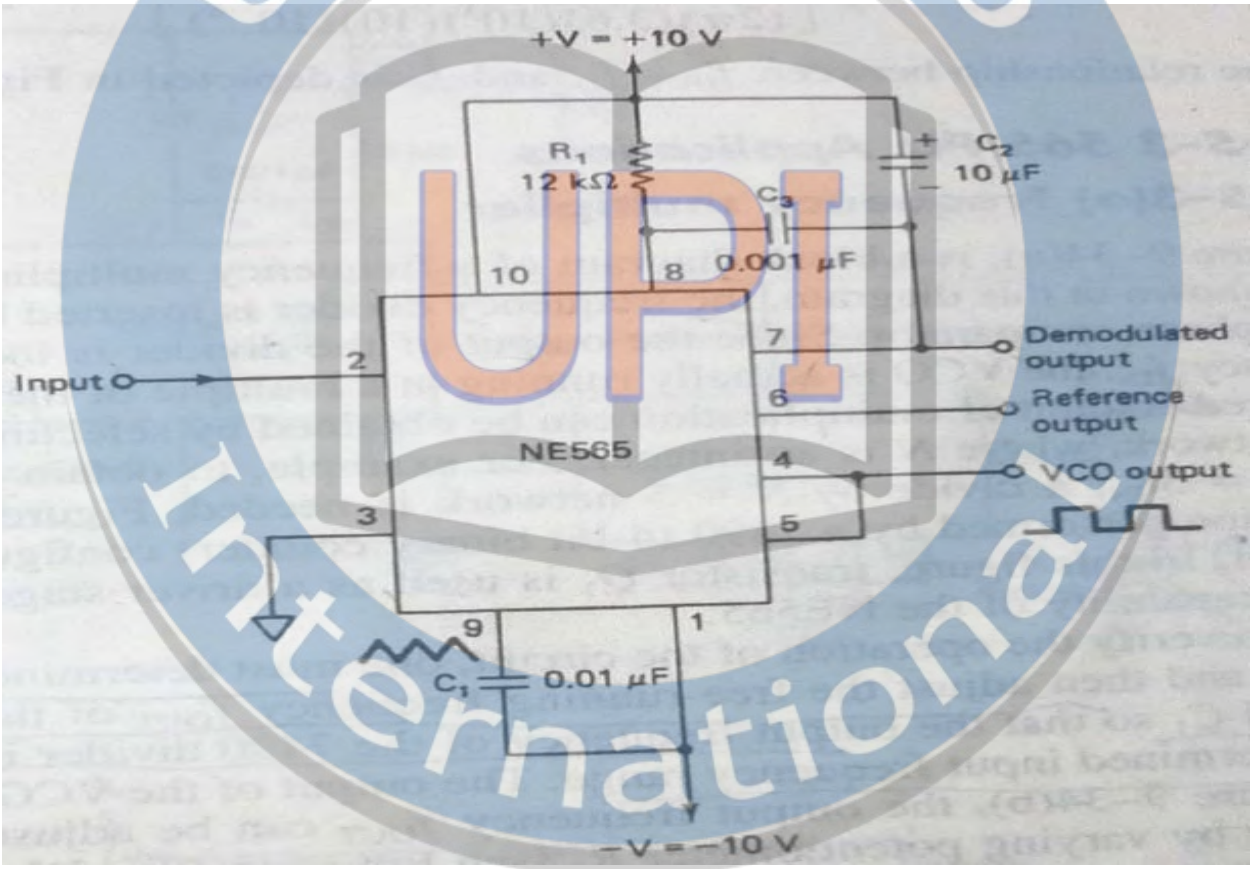
OR

5 (a) Referring to the circuit shown below: (i) Determine the free running frequency f_{OUT}. (ii) The lock range f_L. (iii) And the capture range f_C.



(b) Write any two applications of 565 PLL with block diagrams.

UNIT – III

6 (a) With the help of function table and circuit diagram explain the CMOS 2-input AND gate.

(b) With the help of transition time, propagation delay and power dissipation, explain CMOS dynamic electrical behavior.

OR

7 Write note on advantages and disadvantages of ECL. Through basic ECL inverter/buffer circuit when input is under HIGH and LOW, explain the principle of an Emitter-Coupled Logic (ECL/CML).

UNIT – IV

8 Explain structural, data flow and behavioral modeling styles of VHDL with suitable examples.

OR

9 Write a VHDL program for a prime-number detector using

(a) Structural modeling style. (b) Process-based dataflow modeling style.

UNIT – V

10 With the help of the truth table, explain the logic diagram of a MSI 74x138 3-to-8 binary decoder and model the same using data flow-style VHDL program.

OR

11 What is universal shift register? Draw the truth table, logic diagram of a standard MSI 74x194 4-bit, Universal Shift Register and model the same using data flow-style VHDL program.

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