Code: 15A04306 **R15**

B.Tech II Year I Semester (R15) Regular & Supplementary Examinations November/December 2017

DIGITAL LOGIC DESIGN

(Common to CSE and IT)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) If $4_5 + 2_5 = X_{10}$, then X is

(b) What is meant by canonical form?

(c) Implement AND gate using only two input NOR gates.

(d) What is the importance of don't care condition?

(e) How to perform addition using adder?

(f) What is the working principle of decoder?

(g) Draw the logic circuit of flip-flop and truth table using NAND gates.

(h) What is the function of register? Explain.

(i) A PLA is similar to ROM in concept? Yes or No? How? Why?

(j) How can you perform error detection and correction?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Convert the following to decimal and then to binary: (i) 1101_{16}. (ii) $ABCDE_{16}$.

OR

3 Obtain the dual of the following Boolean expressions:
(i) AB + A(B+C) + B'(B+D). (ii) A + B + A' B'C.

UNIT – II

4 Simplify' the following Boolean expressions using K-map and implement them using NAND gates.
F(W, X, Y, Z) = XZ + W'XY' + WXY + W'YZ + WY'Z

OR

5 Simplify the following expression using tabulation technique:
F = ∑m(0, 1, 2, 8, 9, 15, 17, 21, 24, 25, 27, 31)

UNIT – III

6 Design a 4-bit binary-to-Gray code converter.

OR

7 With the help of a logic diagram and a truth table, explain a 3-line to 8-line decoder.

UNIT – IV

8 Design a 2-input 2-output detector which produces an output 1 every time the sequence 0101 is detected. Implement the sequence detector using JK flip-flops.

OR

9 Design a synchronous 3-bit up-down counter using JK flip flops.

UNIT – V

10 Explain detail about PAL and PLA.

OR

11 Write detailed notes on ECL.

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