Code: 15A04302 **R15**

B.Tech II Year I Semester (R15) Regular & Supplementary Examinations November/December 2017

SWITCHING THEORY & LOGIC DESIGN

(Common to ECE & EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Convert decimal 153 to octal.
(b) Give the associative law and commutative law.
(c) What is prime implicant? How to obtain it?
(d) What are don't-care conditions? What is the use of these?
(e) What is a decoder?
(f) Draw the block diagram of 2-to-1 line multiplexer.
(g) Define synchronous sequential circuit and an asynchronous sequential circuit.
(h) Define flip-flop. List different types of flip-flops.
(i) List different types of ROM.
(j) Compare ROM and RAM.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction: (i) X – Y. (ii) Y - X by using 2's complements.

(b) Obtain the 1's and 2's complements of the following binary numbers:
(i) 00010000. (ii) 00000000.
(iii) 11011010. (iv) 10101010.
(v) 10000101. (vi) 11111111.

OR

3 (a) Simplify the following Boolean functions to a minimum number of literals.
(i) $x(x' + y)$. (ii) $x + x'y$. (iii) $(x + y)(x + y')$.
(iv) $xy + x'z + yz$. (v) $(x + y)(x' + z)(y + z)$.

(b) Find the complement of the functions: $F_1 = x'yz' + x'y'z$ and $F_2 = x(x'y' + yz)$.

UNIT – II

4 (a) Simplify the Boolean function: $F(x, y, z) = \sum(0,2,4,5,6)$.

(b) Simplify the Boolean function: $F = A'B'C' + B'CD' + A'BCD' + AB'C'$.

OR

5 (a) Implement the following Boolean function with NAND gates: F (x, y, z) = (1, 2, 3, 4, 5, 7).

(b) Implement Ex-OR function using only: (i) NAND gates. (ii) NOR gates.

UNIT – III

6 Illustrate the design procedure by taking BCD to excess-3 code converter as an example.

OR

7 (a) Implement full adder with two half adders and an OR gate.

(b) Design Four-bit magnitude comparator gate level circuit.

UNIT – IV

8 (a) With the help of circuit diagram, graphic symbol and characteristic table, explain the JK flip-flop.

(b) Design a four-bit binary Ripple Counter using D flip-flops and then explain the same.

OR

9 Design a Zero-Detector by giving circuit diagram, state table and state diagram.

UNIT – V

10 (a) Explain the architecture of PLA

(b) Briefly introduce the content addressable memory.

OR

11 (a) Explain the architecture of FPGA.

(b) Briefly discuss Flash memories.

*****