Code: 15A05402 **R15**

B.Tech II Year II Semester (R15) Regular & Supplementary Examinations May/June 2018

COMPUTER ORGANIZATION

(Common to CSE & IT)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Compare and contrast RISC & CISC.

(b) What are the basic functional units of a computer?

(c) Perform the subtraction operation for the following numbers: $(63)_{10}$ and $(-17)_{10}$.

(d) What is meant by bit pair recoding? Give an example.

(e) Differentiate static and dynamic memory.

(f) Compare hit rate and miss rate.

(g) How does the processor handle an interrupt request?

(h) Differentiate synchronous bus and asynchronous bus.

(i) What is meant by RAW hazard and WAW hazard?

(j) Mention few interconnection networks that are commonly used in multiprocessors.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Give a short sequence of machine instructions for the task: "Add the contents of memory location A to those of location B, and place the answer in location C." Instructions load LOC, R_i and store R_i LOC are the only instructions available to transfer data between the memory and general purpose register R_i. Do not destroy the contents of either location A or B.

OR

3 Discuss about the various types of addressing modes with examples in detail.

UNIT – II

4 Multiply the following unsigned numbers using Booth's algorithm: Multiplicand = 1000, multiplier = 0011.

OR

5 Draw the organization of the typical hardwired control unit and explain the various functions performed by the various blocks.

UNIT – III

6 A digital computer has a memory unit of 64K*16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. How many bits are there in the tag, index, block and word fields of the address format? How many blocks can the caches accommodate?

OR

7 Discuss how the virtual address is converted into real address in a paged virtual memory system with a neat sketch.

UNIT – IV

8 Exemplify the use of vectored interrupts in processes. Why priority handling is desired in interrupt controllers? How does the different priority scheme work?

OR

9 Draw the typical block diagram of a DMA controller and explain how it is used for direct data transfer between memory and peripherals.

UNIT – V

10 Exemplify how pipeline helps to speed up the processor. Discuss the types of hazard that have to be taken care of in a pipelined processor.

OR

11 What is the purpose of parallel processing? Categorize and discuss the various forms of parallel processing with a neat sketch.

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