

13004**M.C.A DEGREE EXAMINATION DECEMBER 2015
I SEMESTER****PAPER IV: COMPUTER ORGANIZATION
(No additional sheet will be supplied)****Time : 3hours****Max Marks : 75****PART _ A (5x3=15 marks)****Answer any FIVE questions.****Each question carries THREE (3) marks.****Each answer should not exceed ONE (1) page.**

1. Derive the expression for full subtractor? And draw the logic diagram
2. Given a 32 x 8 ROM chip with an enable input , show the external connection necessary to construct a 128 x 8 ROM with four chips and a necessary decoder
3. Derive the circuits for a 3-bit parity generator and 4-bit parity checker using an even-parity bit.
4. It is necessary to transfer 256 words from a magnetic to a memory section starting from address 1235. The transfer is by means of DMA, give the initial values that the CPU must transfer to the DMA controller and give the step by step account of the actions taken during the input of the first two words.
5. Convert the following numerical arithmetic expression in to reverse polish notation and show the stack operation for evaluating the numerical result.

$$3*4[10+2*6/3]$$

6. Distinguish between isolated I/O and Memory mapped I/O
7. A virtual memory has a page size of 1K words. There are eight pages and four blocks. The associative memory page table contains the following entries

Page	block
0	3
1	1
4	2
6	0

Make a list of all virtual addresses that will cause a page fault if used by the CPU

8. What is the cache coherence? Why it is important in shared- memory multiprocessor systems

PART – B (4x15=60 marks)**Answer ALL questions.****Each question carries FIFTEEN (15) marks.****Each answer should not exceed SIX (6) pages.**

9. (a) Simplify the following expression in (1) sum-of-products form and (2) product-of-sums form

$$AC' + B'D + A'CD + ABCD$$
- (b) Design a combinational circuit with three inputs x, y, z and three outputs A, B,C. When the binary inputs is 0,1,2 or 3 the binary output is one greater than the input. When the binary input is 4,5,6 or 7 the binary output is one less than the input.

(OR)

- 10.(a) Design a 2-bit count –down counter. This is a sequential circuit with two flip-flops and one input x. when x=0 the state of the flip-flops does not change. When x=1 the state sequences is 11,10,01,00,11 and repeat.

[P.T.O]

- (b) Simplify the Boolean function F together with the don't – care condition d in product-of-sums form.

$$F(W,X,Y,Z) = \sum(0,1,2,3,7,8,10)$$

$$D(W,X,Y,Z) = \sum(5,6,11,15)$$

- 11 (a). What do you understand about the Assembly language and Assembler? Explain about the first and second pass of the assembler in detail.
- (b). Write an assembly language program to Multiply two positive number with relevant flow chart and comments.

OR

- 12 (a). What is the function of Address Sequencer? Explain the microprogram sequencer for a control memory with neat sketch
- (b) Write a symbolic microprogram of AND logical with the op-code 0100, in control memory with address bus size of 7-bit.

- 13 (a). What are different types of organizations are there explain briefly? Explain about General Register organization with a neat sketch.
- (b). Explain about different types of Instruction formats. Write a program to evaluate the arithmetic statement in different instruction formats

$$X = \frac{A-B+C*(D+E-F)}{G+H*K}$$

OR

- 14 (a). What are the different transfer methods between system and I/O devices? Explain in detail about Asynchronous data transfer techniques in details with relevant timing diagrams.
- (b). Explain in detail of data transmission and receiving by UART with neat sketch
- 15 (a). What do you understand about CAM? Explain in detail internal working principal and matching logic with neat sketch?
- (b). What do you understand about locality of reference? What do you understand about mapping and explain different mapping schemes used in locality of reference memory with neat sketch?

OR

- 16 (a). What do you understand about the multiprocessor? Explain different interconnection structures for multiprocessors.
- (b). What do you understand about the arbitration? Explain hardware and software arbitration methods used in multiprocessors systems